Low-distortion switched-capacitor event-driven analogue to-digital converter

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An event-driven tracking analogue-to-digital converter (ADC) architecture is proposed. The proposed architecture has less sensitivity to amplifier and DAC nonlinearity, and reduces the swing and dynamic common-mode range requirement of the operational transconductance amplifier and comparators, respectively. The efficiency of the ADC is confirmed by detailed circuit simulations.

Introduction: Emerging ultra-low-power applications such as wireless sensor networks and wireless body area networks require the integration of very efficient signal processing techniques, specifically in analogue-to-digital conversion. General-purpose ADCs that rely on Nyquist theory result in unnecessary sampling, and dissipate excessive power within the ADC and subsequent digital signal processing units during periods of low activity. Activity dependent [1], variable resolution [2] ADCs, and continuous time digital signal processing [3] are the most recent techniques to tackle the aforementioned issues. This Letter presents an event-driven ADC architecture, which enables a significant relaxation of the analogue circuit specifications and improvement of the performance.

Event-driven converters: The architecture of an event-driven converter is shown in Fig. 1 [1]. The input signal is scaled-up through a low-noise driver amplifier to the ADC input dynamic range, and is compared with discrete outputs of the resistor string DAC (RSDAC). At each level-crossing event, the output of the RSDAC is increased or decreased by a voltage step of V_{LSB} equivalent to one least significant bit (LSB) of the ADC, always keeping the input signal within a voltage interval defined by the RSDAC outputs V_{up} and V_{down} and which has a magnitude equal to one V_{LSB}. Thus, the tracking accuracy is defined by the RSDAC resolution. Since sampling is not employed in the conversion process, the architecture is very robust to out-of-band interferers, which mitigates the need for an aggressive anti-aliasing filtering and helps to reduce the system total power consumption. However, the circuit implementation of this architecture suffers from several drawbacks. Since the input signal is processed by a low-noise amplifier (LNA), a linear and large output swing LNA is required, which is not straightforward to design in low-voltage regimes. Moreover, rail-to-rail input-stage comparators are necessary to handle the large amplitude signals (large common-mode variation) at the comparator inputs. Finally, the architecture is susceptible to the mismatch of the unit elements of the RSDAC, which may cause in-band harmonic distortion.

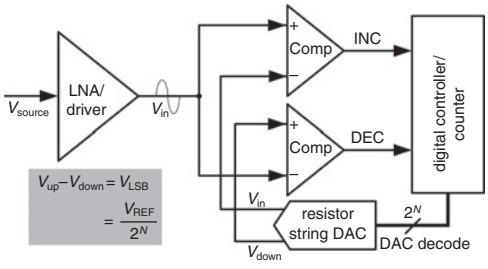

Fig. 1 *Conventional event-driven converter*

Low-distortion event-driven converter: The proposed architecture is shown in Fig. 2. The digital controller and RSDAC of Fig. 1 are replaced with an up/down analogue counter, a switched-capacitor (SC) integrator, and the feedback signal is referred to the input of the LNA. Thus, the LNA processes the tracking error, i.e. quantisation noise, instead of the input signal. Consequently, the signal swing at the output of the LNA is dramatically reduced and is limited to one V_{LSB} in a single-ended design, relaxing the linearity requirement of the LNA [4]. Moreover, the slew-rate requirement of the LNA is considerably mitigated owing to the reduced voltage swing. The integrator, subtractor and LNA enclosed in the dashed box are implemented using a single OTA, i.e. without any additional active element. Since subtraction is performed at the input of the LNA instead of the inputs of the comparators, the comparison is conducted with respect to fixed reference voltages, i.e. not with respect to the dynamic outputs of the RSDAC. Removing the dynamic common-mode voltage at the input of the comparators, rail-to-rail input-stage comparators are not required, which helps to reduce the power consumption. The nonlinearity issue of the multi-bit RSDAC is resolved by using a single-bit SC integrator, which is controlled by clock phases generated by comparator output increment (INC) and decrement (DEC) signals. A continuous-in-time and discrete-in-amplitude output is obtained using an asynchronous Gray-code up/down counter, which also minimises any potential error in consecutive synchronous sampling for spectral analysis purposes.

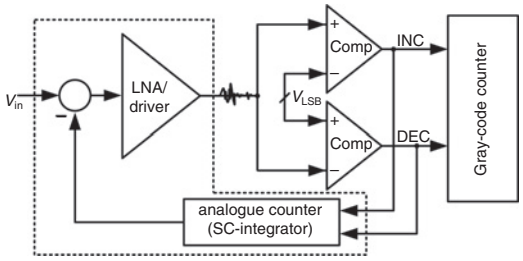

Fig. 2 *Proposed event-driven converter*

Circuit implementation: The circuit implementation of the proposed architecture and its corresponding timing diagram covering several consecutive crossing events is shown in Fig. 3. A fully differential realisation is employed, but a single-ended view is shown for the sake of simplicity. The continuous-time signal path formed by C_1 and C_2 provides additional gain for the input signal. The subthreshold diode-connected transistors in the feedback path provide the input common-mode voltage of the LNA, in long periods of signal inactivity. The integrator is realised by means of two time-interleaved capacitors C_2, which are controlled by non-overlapping phases of φ_1 and φ_2 as a way to relax the bandwidth requirement of the LNA, and at the cost of a negligible penalty related to the mismatch between two capacitors. It can be shown that the residue of the error at the LNA output, which is due to the mismatch of the two capacitors, integrates to zero for two consecutive INC or DEC crossing events, and is bounded to a maximum of one V_{LSB} for consecutive INC and DEC events, which occurs at zero input signal. The resolution of the ADC is adjusted by tuning parameter k or V_{LSB}. Differential comparators detect the crossing events. The DEC and INC signals are generated using the same differential reference voltages as in the integrator. Comparator offsets are cancelled by isolated DC operating points provided by highpass filtering in front of the comparators [1]. At each crossing event, the DFF generates an integration phase which is valid until the next crossing event in order to utilise the entire timing slot between two consecutive events for linear settling of the integrator. A conventional non-overlaping phase generator is used to generate non-overlapping integration phases φ_1 and φ_2 and the corresponding up/down integration phases $\varphi_{1u,d}$, and $\varphi_{2u,d}$, respectively.

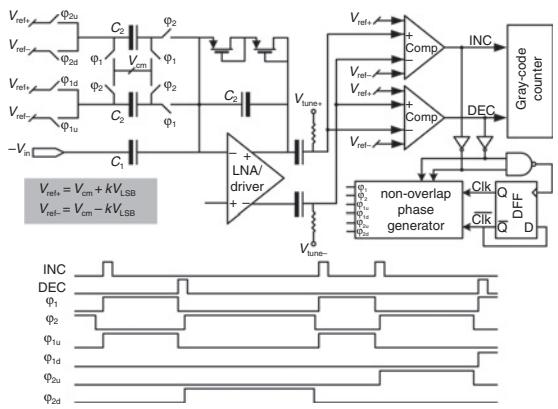

Fig. 3 *Circuit implementation and corresponding timing diagram of proposed architecture*

Simulation results: The proposed structure has been simulated using a 0.18 μm CMOS technology with a 1.8 V supply voltage. The ADC can handle a full scale of 1 V_{p-p} (0 dBFS) single-tone input signal up

to a frequency of 1.8 kHz without slope overloading and a total static current consumption of 6.8 μA. The higher input frequencies are processed with smaller amplitudes, e.g. −6 dBFS at 3.9 kHz. The output spectrum and dynamic range (DR) plot of the 8-bit ADC using an OTA with 31 dB of DC gain is shown in Fig. 4. Synchronous sampling at 250 kHz at the output of the Gray-code counter is used for spectral analysis purposes. The spurious free dynamic range (SFDR) with 0 dBFS input is simulated at 52.1 dB without considering any mismatch between the time-interleaved capacitors C_2, and slightly degrades to 50.4 dB by introducing the 3% of mismatch. The signal-to-quantisation-noise ratio (SQNR) integrated up to a frequency of 15.625 kHz is 46.8 and 45.8 dB without and with C_2 mismatch, respectively. The DR of the ADC is simulated at 48.6 dB. Better SQNR performance may be achieved by continuous-time filtering-out-of band components prior to synchronous sampling.

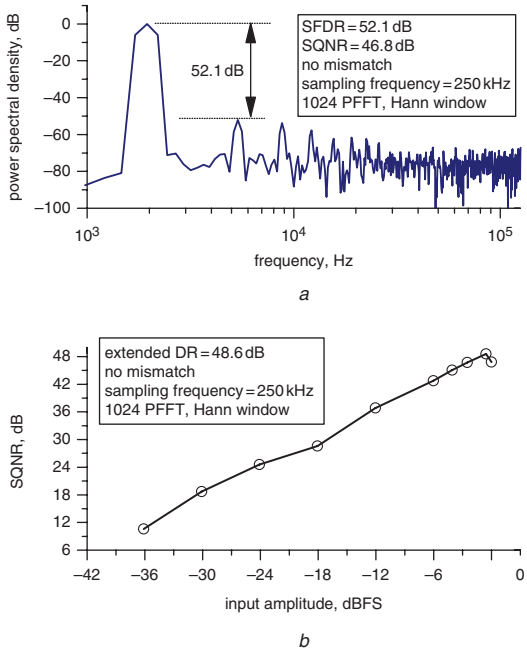

Fig. 4 *Output spectrum of ADC and DR of ADC after synchronous sampling*
a Output spectrum of ADC
b Dynamic range of ADC

Conclusion: A clock-less tracking low-distortion ADC is presented. Simulation results of the ADC prove the robustness of the architecture with respect to analogue circuit non-idealities, at low static power dissipation.

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One or more of the Figures in this Letter are available in colour online.

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